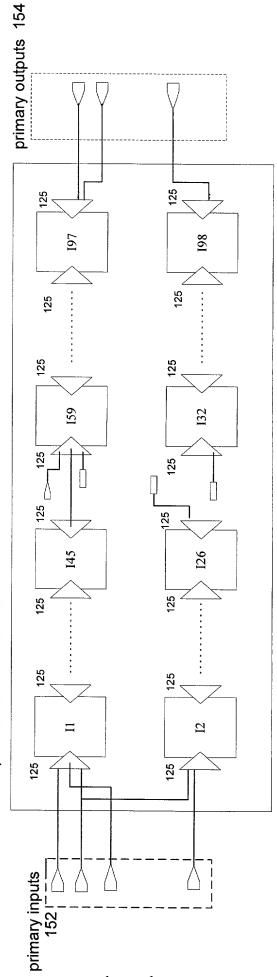
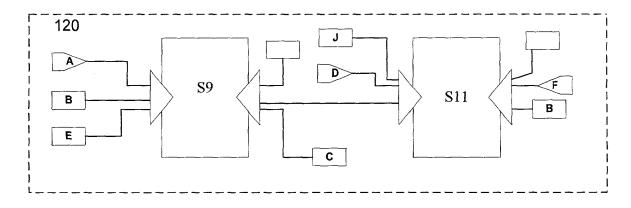
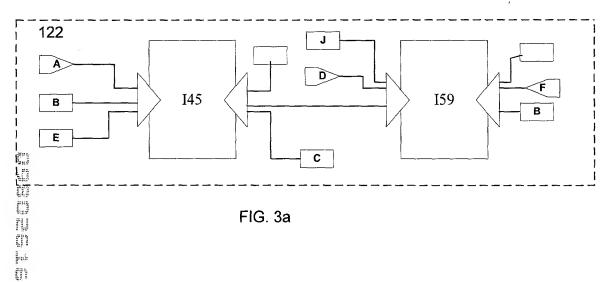


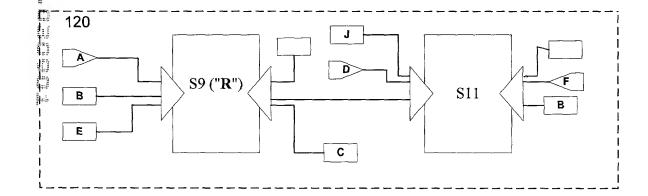
implementation circuit 122





STAGE 1





STAGE 2

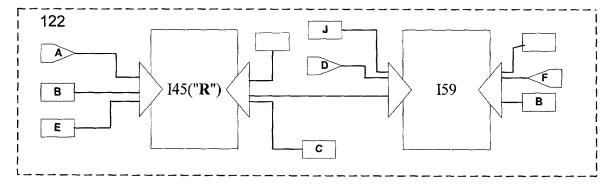
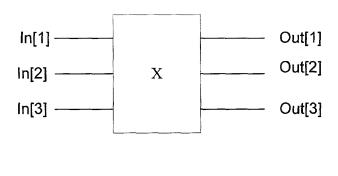
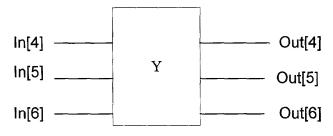


FIG. 3b

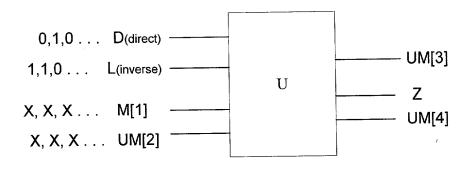
FIG. 4

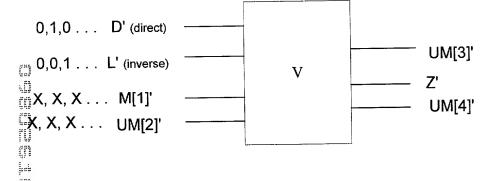
Fanin signatures		Fanout	Fanout signatures		
ABE	DJ	C	BF		
<b>S</b> 9	S11	S9	S11		
<i>I45</i>	159	I45	<sup>4</sup> I59		
	S7	S57	S29		
***	135	I14	I8		
	{	S80	S64		
		126	I53		
	······································	I75	3		
		I76	1		
		***************************************			
1			;		
f" *	· · · · · · · · · · · · · · · · · · ·				
Fanin s	signatures	Fanout	signatures		
Fanin s	signatures DJR	Fanout C	signatures BF		
ABE	DJR	С	BF		
ABE S9	DJR <b>S11</b>	C S9	BF S11		
ABE S9	DJR <b>S11</b>	C S9 I45	BF S11 159		
ABE S9	DJR <b>S11</b>	C S9 I45 S57	BF S11 I59 S29		
ABE S9	DJR <b>S11</b>	C S9 I45 S57 I14	BF S11 I59 S29 I8		
ABE S9	DJR <b>S11</b>	C S9 I45 S57 I14 S80	BF S11 I59 S29 I8 S64		
ABE S9	DJR <b>S11</b>	C S9 I45 S57 I14 S80 I26	BF S11 I59 S29 I8 S64		
ABE S9	DJR <b>S11</b>	C S9 I45 S57 I14 S80 I26 I75	BF S11 159 S29 18 S64 153		





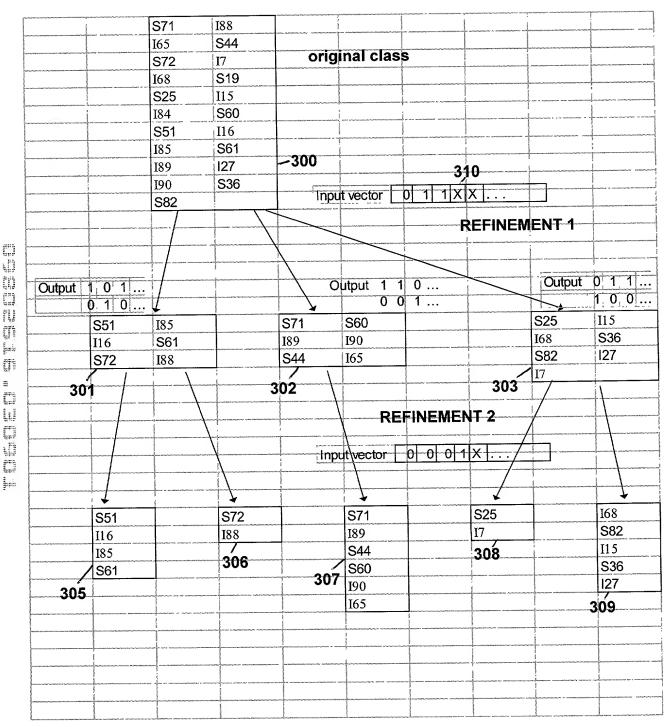
250	In[1]	In[2]	in[3]	Out[1]	Out[2]	Out[3]
Y	0	0	0	0	1	0
	0	0	1	1	1	1
	0	1	0	0	1	1
Don't care input	0	1	1	1	0	1
	1	0	0	0	0	0
Don't care input	1	0	1	1	0	1
	1	1	0	1	1	0
	1	1	1	0	1	0
			,,,		,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	
255	In[4]	ln[5]	In[6]	Out[4]	Out[5]	Out[6]
	0	0	0	0	1	0
	0	0	1	1	1	1
······································	0	1	0	0	1	1
Don't care input	0	1	1	0	1	1
***************************************	1	0	0	0	0	0
Don't care input	1		1	0		1
Don't care input	1	0	į .	, .	, ,	5
Don't care input	1	1	0	1	1	
Don't care input	1	1 1 1	, 0 1	1 0	1	





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	D	L	D'	L'	M[1]	M[1]'	UM[1]	UM[1]'	Z	Z
1	0	1	0	0	X	Χ	Χ	X	0	1
2	1	1	1	0	X	X	Χ	Χ	1	0
3	0	0	0	1	X	X	X	X	0	1
•					<b>~~</b>					
•										
30	1	10	1	1	X	X	X	Χ	0	1
31	'n	1	0	0	X	Χ	X	Χ	0	1
32	1	0	1	1	X	Χ	X	X	X	X



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FIG. 8

